Chapter 2

CMOS Micromachining and MEMS Design Packages

CMOS micromachining is a combination of the standard CMOS process and silicon micromachining technology. First, the standard CMOS process is used to build a MEMS structure with electric circuitry on a silicon substrate. An opening is created on the substrate by making all the films absent in that region. Afterwards, isotropic or anisotropic etching is used to release the MEMS structure. In this chapter, a typical CMOS micromachining fabrication process is described to illustrate the general procedure of fabricating CMOS micromachined devices.

Since micromachining fabrication technologies are borrowed from the microelectronics industry, IC design packages are naturally used for MEMS design. In recent years, some design packages focusing on MEMS designing, e.g. MEMS Pro from MEMSCAP® Inc. (headquarters: St. Ismier, France and Oakland, CA, USA), have been developed. In this chapter, MEMS design strategies along with the MEMS design packages available to Canadian universities through the Canadian Microelectronics Corporation (CMC) are briefly introduced and compared on the basis of the criteria such as working environment, ease of use, etch simulation and design rule checking.

2.1 A typical CMOS micromachining process

Figure 2.1 shows a cross-section of a MEMS structure built with the Mitel 1.5 μm process and with all the layers present.

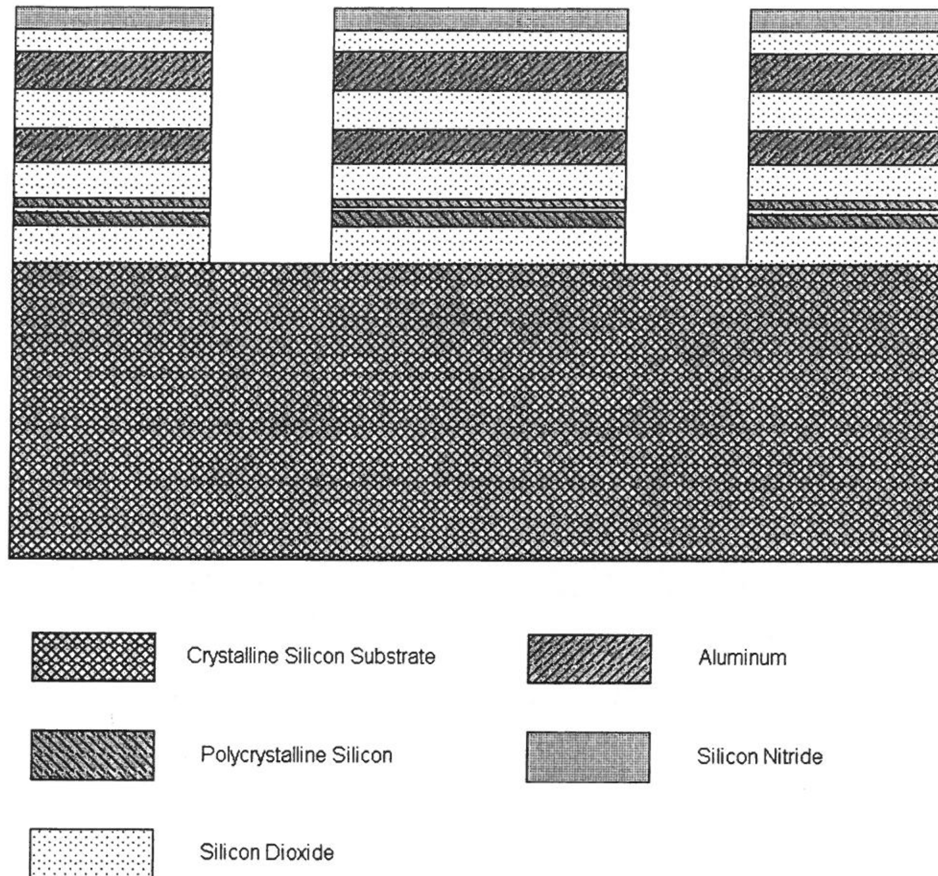

Figure 2.1 Cross-section of a wafer of a typical CMOS micromachining fabrication (not drawn to scale)

A typical Mitel 1.5 μm CMOS micromachining fabrication process may include the following steps.

- Highly conductive n+ doped layers are diffused over the n-type silicon wafer.
- A 0.9 μm field oxide layer may be used as a dielectric layer which electrically isolates the polysilicon structure from the crystalline substrate. It may also be used as structural material.
- After the field oxidation and gate oxidation (about 0.027 μm, not shown in Figure 2.1), two layers of low-stress, doped polysilicon are then deposited (about 0.32 μm and 0.25 μm thick, respectively) with a 0.02 μm oxide layer between. The polysilicon layers can also be used as electrically conductive layers.

- Then a 0.8 μm dielectric layer mainly composed of low-stress phosphosilicate glass (PSG) is deposited.
- Two 0.8 μm patterned aluminum layers are then used to form conducting layers and electrical interconnects. There is a 1.0 μm inter-dielectric oxide layer between two metal layers.
- Finally, two layers of passivation (0.5 μm oxide and 0.5 μm nitride) are deposited.

After the MEMS structures are fabricated, etching of the silicon substrate is used to release the structure from the substrate. There are two different types of etching: anisotropic and isotropic etching. Anisotropic etching is a process of preferential directional etching of material using liquid etchants like Ethylene Diamine Pyrocatechol (EDP) or Tetra Methyl Ammonium Hydroxide (TMAH). Isotropic etching refers to the etching of material regardless of crystallographic-orientation using an etchant such as Xenon difluoride.

Xenon difluoride has come into use as a replacement for anisotropic etchants EDP and TMAH recently [1-4] because of safety considerations. Xenon difluoride is a white solid at room temperature and pressure and sublimates at a pressure of about 500 Pa. Xenon difluoride vapor can etch silicon isotropically without external excitation and it has extremely high selectivity to many materials commonly used in MEMS.

The overall silicon/xenon difluoride reaction equation is given by:

$$2XeF_2 + Si \rightarrow 2Xe + SiF_4 \tag{2.1}$$

The reaction is exothermic and the main product SiF_4 is volatile at room temperature. It should be noted that moisture on the chip, which causes HF formation with exposure to XeF_2 gas, is a safety hazard to operating personnel and can also result in silicon dioxide etching.

Figure 2.2 is a schematic picture showing the CMOS micromachined structure in Figure 2.1 isotropically released from the substrate. The actual shape of the etched cavity and the roughness of the etched surfaces depend on the amount of undercutting, the ease of circulation of XeF_2, etc.

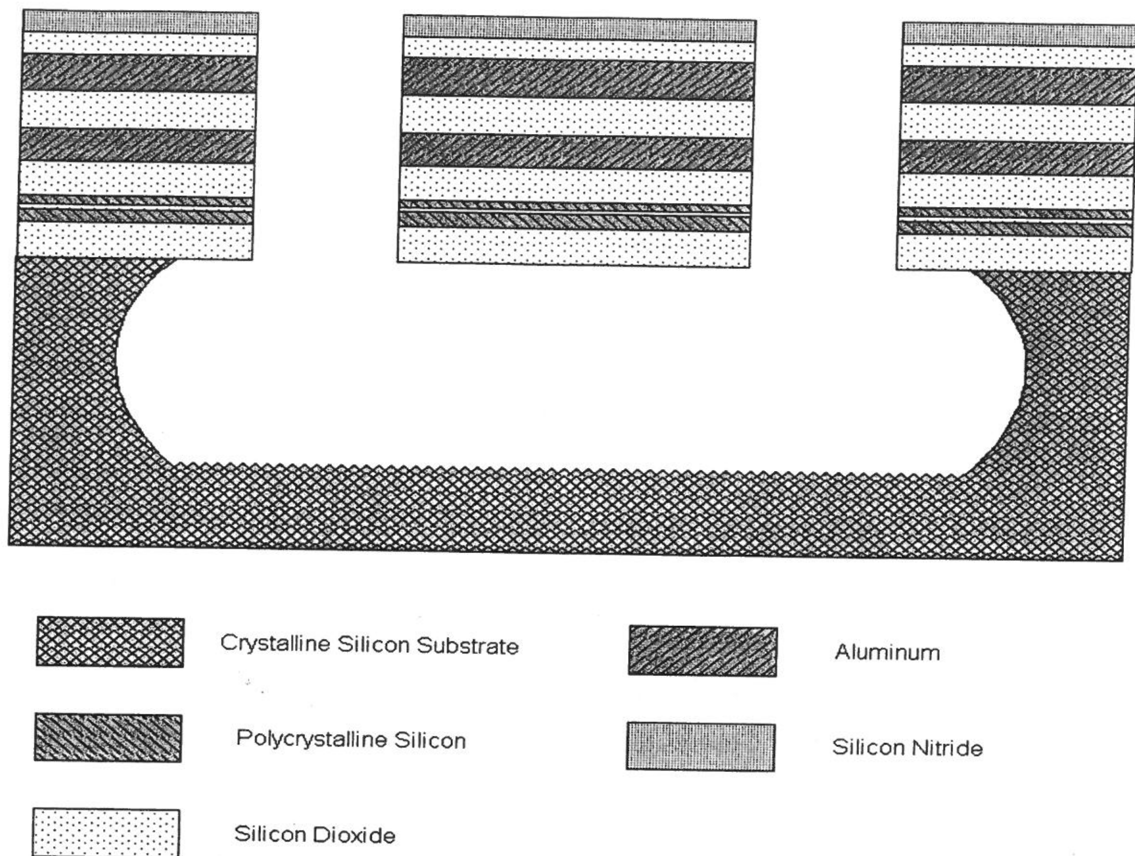

Figure 2.2 Cross-section of a typical MEMS structure released with XeF_2

2.2 MEMS design packages

There are two different MEMS design strategies: the system approach and the device approach. The system approach starts from a schematic, which uses symbols or hardware description language (HDL) models to build the system. The schematic is then simulated and mask layout is generated for fabrication. The device approach starts directly from a mask layout, which is a scaled layer-by-layer drawing of the MEMS structures. Different colors are used to represent different layers of the structure. Finite element analysis (FEA) software, such as ANSYS, can be used to simulate the device by transferring the mask information directly into the FEA software to build the model for simulation.

There is an increasing interest in hardware description languages recently because of the rapid increase in circuit complexities, an industry-wide desire for more formal (correct-by-design) engineering methods, and a general maturing of low-cost, more accessible HDL tools [5]. HDL models convert mechanical systems to equivalent electrical models. However, the HDL models are limited to systems that are simple enough to be described by closed-form equations. All the design related to this project used the device approach.

There are three software packages currently used in the universities for IC and MEMS design: Cadence, Mentor Graphics and MEMS Pro. The advantages and disadvantages of each of the software packages are discussed below from the design experience of the author.

2.2.1 Mentor Graphics MEMS design kit

A CMP® (Circuits Multi-Projects, Grenoble, France) / Mentor Graphics MEMS design-kit was used and evaluated for about one year under a contract with CMC [6].

The kit was installed on a Sun workstation running the Solaris operating system. Learning Mentor Graphics proved to be challenging, especially for new users who had no previous experience with Mentor Graphics and HDL modeling. The design kit provides a system design possibility using HDL simulation tools within the package. However, as mentioned above, it is only appropriate to MEMS structures simple enough to be described by a closed form equation, which then can be converted to its electrical "equivalent".

The package also has a cross-sectional viewer and an etch simulator. The cross-sectional viewer provides the user with a feel for the three dimensional representation of the object under design. The etch simulator gives the user a view of the released device after etching. However, the etch simulator gives reasonable predictions for simple structures, but not for more complex structures like the Cantilever-In-Cantilever [7]. The design rule checker provided with Mentor Graphics MEMS design kit proved to be adequate.

In general, the package is satisfactory for designing MEMS devices. It is neither significantly better nor worse than other MEMS design packages.

2.2.2 Cadence IC layout editor and Multi-User MEMS Processes (MUMPs) design kit

Cadence does not have a package for general MEMS design; the layout editor for IC design is used for mask design. Cadence uses the Solaris operating system. Design can only be implemented from the device approach.

The IC layout editor has many useful functions for object editing and learning to use it is relatively straightforward. It does not have any MEMS-related functionality like a cross-sectional viewer or etch simulator. However, Cadence has a Multi-User MEMS Processes (MUMPs) design kit available through CMC for surface micromachining design using the MUMPs technology of JDS Uniphase Inc. – MEMS Business Unit. The kit has a MUMPs device library, including some commonly used devices like comb drives, and electrostatic motors. Although the MUMPs technology is different to the CMOS technology, the design kit can be used for CMOS micromachining design by modifying its technology file. The design rule checker (DRC) of the kit needs improvement. Some parts of the layout with DRC violations turned out to be fine after fabrication; some parts without DRC violations did not work as expected afterwards.

In general, the layout editor of Cadence and the MUMPs design kit is satisfactory for MEMS and especially MUMPs design. The IC layout editor in Cadence is very convenient for mask design.

2.2.3 MEMSCAP® MEMS Pro

MEMS Pro is a full suite of tools for MEMS and IC design and layout. The package includes schematic entry for IC design, IC circuit simulation and waveform viewing, layout editing, design rule checking and MEMS libraries.

MEMS Pro runs on a PC with Windows 95, Windows 98, or Windows NT 4.0. It needs a Pentium processor or better and 150 MB of disk space.

The layout editor, L-Edit, is originally from Tanner Research, Inc. and is very efficient and easy to use for mask designing. Figure 2.3 shows the design interface of L-Edit with a serpentine-shaped polysilicon resistor as an example. The interface screen can be divided into three parts: the tool palettes on the top of the screen; the layer palette on the left of the screen and the work area, where the polysilicon resistor layout is drawn.

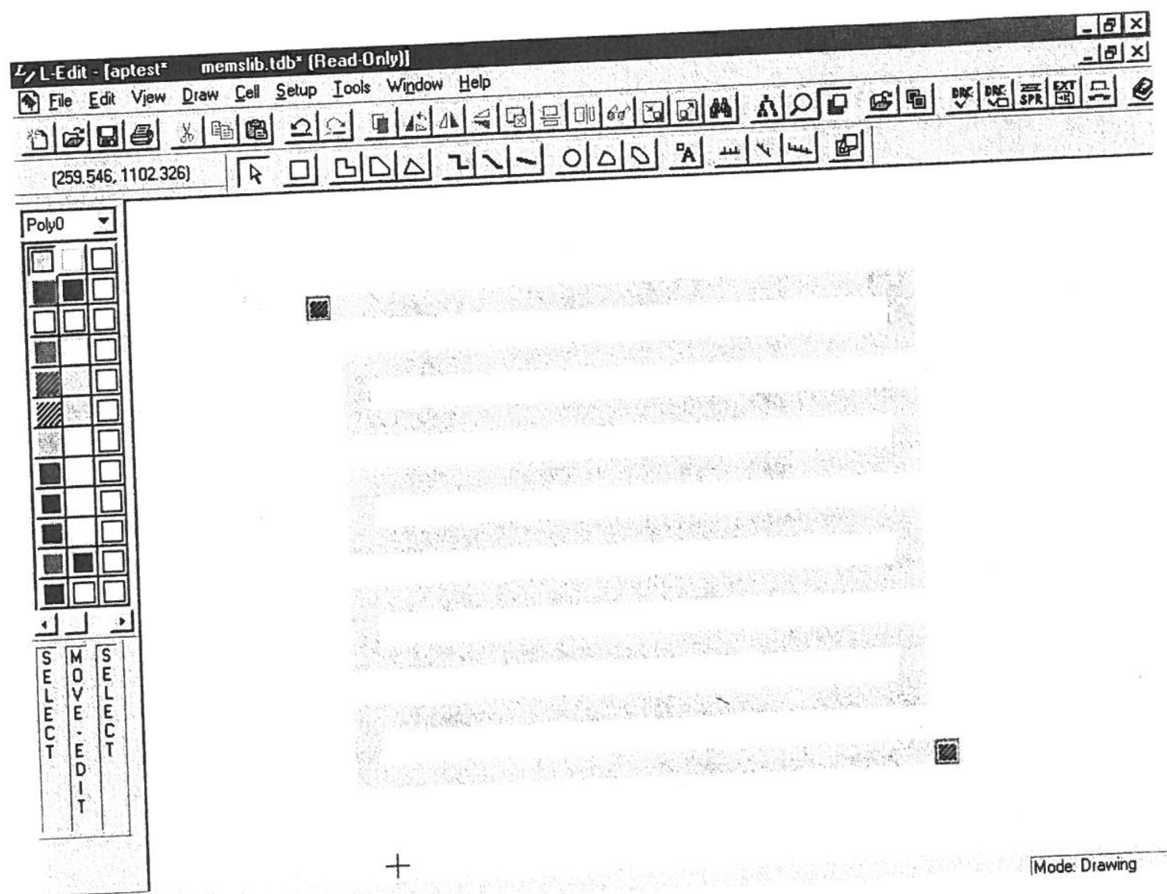

Figure 2.3 L-Edit user interface with a polysilicon resistor layout as an example

L-Edit provides standard shape selection, such as squares, circles and polygons. It also supports all-angle wire placement. The editing of shapes is easy with functionality such as stretch, rotate, flip and emerge. The design rule checker is also adequate.

Comparing the three packages introduced in this chapter, MEMS Pro has the advantage of ease of use and is amply equipped with the most features MEMS designer request. Its operating system is Windows. For designers with a preference for the Solaris operating system or designers with previous IC design experience, Cadence can be the best choice. It should be noted that both MEMS Pro and Cadence do not have an etch simulator by the time of writing this thesis. If the etching profile is critical to the design, a design package equipped with an etch simulator like the Mentor Graphics MEMS design kit will be necessary.

Both MEMS Pro and Cadence have been used in this project for the design and mask layout.

References:

[1] P. B. Chu, J. T. Chen, R. Yeh, G. Lin, J. C. Huang, B. A. Warneke, and K. S. J. Pister, "Controlled Pulse-Etching with Xenon Difluoride", *Ninth Int. Conf. Solid-State Sensors and Actuators (Transducers '97)*, Chicago, June 1997, pp. 665-668.

[2] R. Toda, K. Minami, and M. Esashi, "Thin Beam Bulk Micromachining Based on RIE and Xenon Difluoride Silicon Etching", *Ninth Int. Conf. Solid-State Sensors and Actuators (Transducers '97)*, Chicago, June 1997, pp. 671-674.

[3] F. I. Chang, R. Yeh, G. Lin, P. B. Chu, E. Hoffman, E. J. J. Kruglick, and K. S. J. Pister, "Gas-phase Silicon Micromachining with Xenon Difluoride", *Sym. on microelectronic structures and MEM devices for optical proc. and multimedia appl. (Proc. SPIE 2641)*, October 1995, pp. 117-128.

[4] I. W. T. Chan, K. B. Brown, R. P. W. Lawson, A. M. Robinson, Y. Ma and D. Strembicke, "Gas Phase Pulse Etching of Silicon for MEMS with Xenon Difluoride", IEEE Can. Conf. On Electrical and Computer Engineering, Edmonton, May 1999, pp. 1637-1641.

[5] D. Pellerin, D. Taylor, *VHDL Made Easy*, Prentice-Hall, Inc., London, 1997.